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# How to Implement an Experimental Course on Analog IC design in a Standard Semester Schedule

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**Abstract**— One of the challenges in teaching integrated analog electronics is that it is difficult to offer courses where the students can design, layout and tape-out a circuit and subsequently perform measurements on the device due to the long turn-around time in IC fabrication. In this paper it is described how the sequences of courses in integrated analog electronics at the Technical University of Denmark have been modified to enable this. It is outlined how a course can be designed using the three elements in constructive alignment: intended learning objectives, teaching activities and assessment. As an example it is described in detail how a new course is designed. The course is the first of two new courses and the scope of the course is to teach the students the flow an IC designer has to go through when designing analog circuits. Additionally the course has a large focus on strengthening the generic engineering competences of the students. This is achieved by running the course as a project in a company with status meetings and a review meeting where the teacher acts as a manager. Finally, the course evaluation based on the Course Evaluation Questionnaire (CEQ) is presented and based on this future improvements to the course are discussed.

## I. INTRODUCTION

Analog integrated circuits remain an important part of electronics today, and are practically present in all system-on-chip (SoC). Highly skilled and experienced engineers within integrated circuit design are thus still in high demand.

Integrated circuit design requires a high level of theoretical and analytical skills. However, practical experience is equally important due to vast design space and complex tools. Optimizing circuits using the available Electronic Design Automation (EDA) tools is a craftsmanship, and this requires years of experience to create state-of-the-art circuits.

Today the teaching of analog IC design at universities is most often focused on analytical skills and general circuit theories. The practical aspect is limited to schematic level simulations and possibly layout of circuit blocks. Full synthesis of a circuit, as shown in Fig. 1, including schematic level design, corner simulations, full-circuit layout, design-rule-checking (DRC) and layout-versus-schematic checking (LVS) before tape-out, is not possible to teach in a standard semester course. The multi-project-wafer (MPW) schedule of the foundry and the fabrication time for an IC of typically 3 months makes it practically impossible to incorporate the tape-out of an IC in a standard 13 week semester course. In a master thesis project, carried out over a period of 5 months,

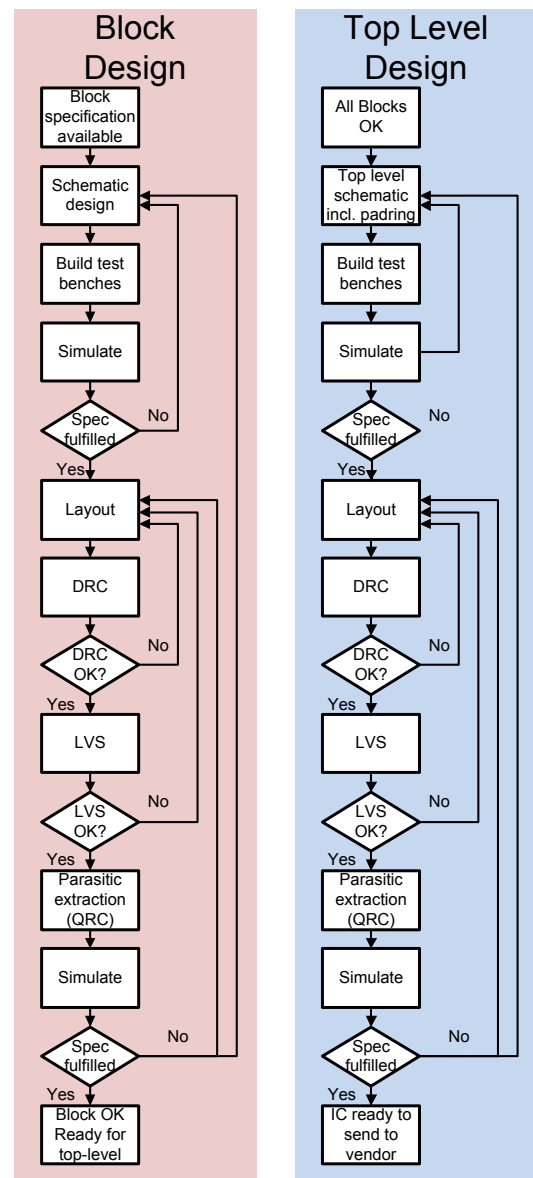


Fig. 1 The flow for analog circuit design and chip assembly.

the same time-constraints apply. Overall this limits the possibility of the student to gain experience with the full design flow of an analog IC during his/her engineering studies.

This paper concerns the design and implementation of a new course specifically aimed at teaching students the practical aspects of analog IC design, and focusing on the full design flow.

The outline of the remaining part of this paper is as follows: In section II is described the planning of the sequence of courses in analog IC design at DTU, incorporating two new practical courses. Section III presents a general strategy for designing courses based on constructive alignment [1], [2]. These strategies are used in section IV for implementing the course “Design and Layout of Integrated CMOS Circuits”, [3]. This section also describes the important aspect of including in the course the development of the students’ general engineering competences [4]. Section V present the students’ learning in the course, based on the Course Experience Questionnaire (CEQ). A conclusion is given in Section VI.

## II. COURSE SEQUENCE AND NEW EXPERIMENTAL COURSES

At the Technical University of Denmark (DTU) a semester is divided into two parts. First, a 13 weeks period mainly used for courses based on one weekly lecture and appertaining exercises followed by examination. The workload in the 13 week period is rated to 25 ECTS (European Credit Transfer System) points where a typical course is rated to 5 ECTS points. Second, after the 13 week examinations a 3 weeks period follows rated to 5 ECTS points. In this period the students typically work full time on a single project.

Up until a year ago no course was offered at DTU where a student had the opportunity to design a circuit on an IC, tape it out and subsequently perform measurements on the designed circuit. As discussed in the introduction the main reason for this being that the processing time for ICs is approximately 3 months, meaning that design of circuitry and tape out cannot be done within the time limits of a normal semester. The original sequence of courses in analog integrated circuit design at DTU is shown at the top of Fig. 2. It consists of two traditional lecture courses in integrated analog electronics [5], [6], a course in circuit synthesis where the students are offered the opportunity to design a circuit (without tape out) [7] and finally the M.Sc. thesis project.

To offer courses where a circuit can be designed and manufactured, two new courses have been created as shown in at the bottom of Fig. 2. The general idea is to separate the two course in time by approximately half a year to enable processing of the ICs in between the two courses. The 3 week period in the 8<sup>th</sup> semester takes place in June and here the first

course “Design and Layout of an Integrated Circuit” [3] is allocated to design and layout an integrated circuit. All designs are assembled on a single chip that is taped out. The fabrication and handling of the IC is then performed in the period between the two new courses and thus the students are able to return for the 9<sup>th</sup> semester 3 week period in January to characterize the design they made. Both courses are rated to 5 ECTS points.

In the period between the two new courses the students are offered the course “Synthesis in Electrotechnology” [7] which is offered in a 5 or 10 ECTS point version. In the course the students agree with a teacher on an individual design tasks in any subject related to electronics. Often this course was used to introduce the students to the design flow of integrated analog electronics but as this is now done in the first of the two new courses more advanced topics can be addressed in this course.

## III. DEVELOPMENT OF A COURSE

Over the last decade there has been an increasing focus on higher learning at universities and a large amount of research has gone into learning how students learn [1], [2]. To design a course many approaches exist and here constructive alignment [1], [2] is used. Constructive alignment uses three elements in the course planning (intended learning objectives, teaching activities and assessment) with the primary focus to increase student learning and competences as illustrated in Fig. 3. In the following the three elements in the course planning is described as a sequential process but in practice it is an iterative process where the three elements are revisited until they are aligned. Also, the three elements should be revised after the final course evaluation to ensure that the student learning and ILOs are aligned.

### A. The Intended Learning Objectives (ILO)

The first step in planning the course is to identify the intended learning objectives (ILO). The ILOs are short statements of what a student will be able to do if they are met, i.e., what one would like the students to learn. For the teacher the ILOs serve two purposes. First, the ILOs greatly help to plan the course and the teaching activities (TA) as they serve as the goal for the teaching. Second, at the end of the course they are also very useful when designing an examination and

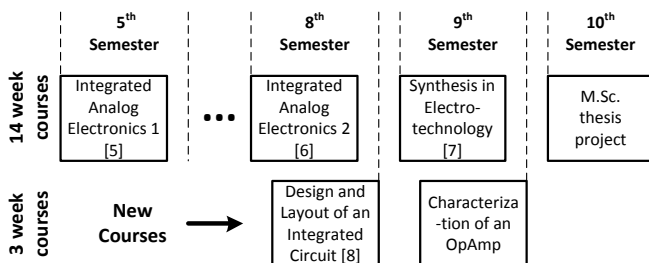


Fig. 2 Recommended course sequence in integrated analog electronics at DTU including two new experimental courses.

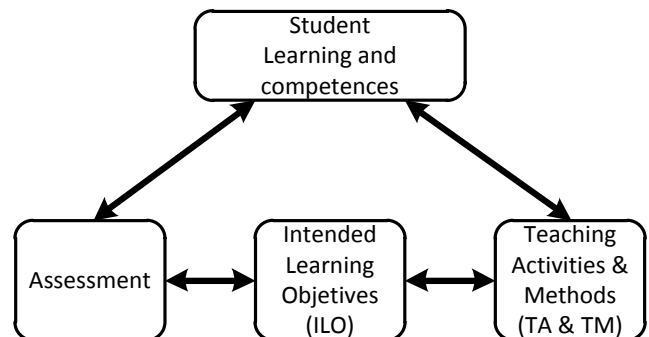


Fig. 3 A model for constructive alignment [1].

finally when assessing the students. When formulating the ILOs it is important to ensure that they address both lower and higher level learning, e.g., according to the SOLO [1] or Bloom's taxonomy [1], [2], [8].

The students also have great use of the ILOs, e.g., in case a written report is the basis for the assessment then the ILOs show the student the topics to cover in the report.

#### B. The Teaching Activities (TA) and Teaching Methods (TM)

Once the ILOs are made the teaching activities (TA) are planned and along with these the teaching methods (TM) are chosen. The TMs are the principles used to teach whereas the TAs are the actual activities planned in the course. The most commonly used TAs at universities are probably lectures, problem solving sessions and project work but they can in principle be anything like excursions, quizzes, etc. A large variety of teaching methods exist, e.g., inductive learning, problem based learning, learning by inquiry etc.

After choosing the TAs and TMs they are mapped against the ILOs to ensure that all ILOs are covered and thereby ensure the basis for student learning.

The TAs and TMs chosen naturally depend on the size of the classes. Classes with a large number of students cannot be taught on an individual basis and thus lectures and problem solving sessions are often used in this situation. Classes with few students offer the opportunity to teach the students individually or in small groups and thereby use many different teaching methods as will be illustrated in the example later in this paper.

#### C. Assessment

Based on the TAs and the ILOs it is decided how the level of formative and summative assessment [1] should be implemented in the course. Here the ILOs again hold a central role for both the students and the teacher. E.g., if a written

examination is prepared one should try to cover all the areas stated in the ILOs and summative grading is typically used. This is in contrast to formative assessment which is better suited for providing the students personal feedback on their learning and generic engineering competences [4].

Finally, part of the assessment is also to decide how to grade the student, i.e., by grades of pass/fail.

#### IV. COURSE PLANNING EXAMPLE

In section II it was described how the sequence of courses has been modified at DTU to provide courses where the students have the possibility to design an integrated circuit, tape it out and perform measurements on it after fabrication. In this section the planning and execution of the first of the two new courses "Design and Layout of an Integrated Circuit" [3] is described in detail.

##### A. Course Vision

The main idea behind the course is for the student to go through the flow of block design as shown in Fig. 1 and fabricate their designs on a chip. Besides teaching the students the flow for IC block design it is also the goal to strengthen the generic engineering competences of the students.

##### B. The Learning objectives

The ILOs, listed in Table I, are formulated to cover the flow for block design as shown in Fig. 1. As part of the flow the students are expected to try all the tools in the EDA software, i.e., using the schematic editor, the simulation environment, the layout editor and the DRC and LVS tool. As something new for the students they are asked to verify their design in all process corners. Due to time limitation in the 3 week course it was decided not to include parasitic extraction as a topic in the course.

The ILOs are formulated using different level of learning

TABLE I. MAPPING OF THE INTENDED LEARNING OBJECTS (ILO) AND THE TEACHING ACTIVITIES (TA).

| Intended Learning Objectives (ILO)  | Teaching Activities (TA) |               |                     |                 |                |
|---|--------------------------|---------------|---------------------|-----------------|----------------|
|   | Lectures                 | Computer Work | Coaching & Guidance | Status Meetings | Review Meeting |
| Synthesis an Operational Amplifier according to a certain specification in a CMOS process                         | x                        | x             | x                   | x               | x              |
| Use a schematic editor and simulation environment for design and analysis of analog circuitry                     | x                        | x             | x                   | x               |                |
| Analyze the performance of the design in all process corners  |                          | x             | x                   | x               | x              |
| Correlate simulated results with calculated value based on a small signal equivalent of the operational amplifier |                          | x             | x                   | x               | x              |
| Use a Layout Editor for making layout of analog circuitry   | x                        | x             |                     | x               |                |
| Identify parts of the design critical to matching and make layout that ensure good matching for these parts       | x                        | x             | x                   | x               | x              |
| Use a DRC tool (Design Rule Checking) to ensure design fulfills design rules                                      | x                        | x             |                     | x               |                |
| Use a LVS tool (Layout Versus Schematic) to ensure the layout matches the schematic design                        | x                        | x             |                     | x               |                |
| Design a simple padding for the design at schematic level   |                          | x             | x                   | x               | x              |
| Document the work in a final report   |                          |               | x                   |                 |                |

ranging from the lower level (e.g. “use” and “identify”) to higher level learning (e.g. “synthesis” and “analyse”). The different levels are used to emphasize that IC design requires a significant portion of craftsmanship and also relies on the systematic analysis and creativity used in the design phase. Also, by defining the ILOs at different levels they enable “not so skilled students” to pass the course while still leaving room for the skilled students to excel.

#### *C. Teaching Generic Engineering Competences using the Company model*

Besides teaching the student the technical and practical aspects of doing analog IC design, the course is also designed to teach the student generic engineering competence [4]. This includes team work, problem solving, presentation technique etc. The generic engineering competences are the non-technical skills needed in a normal working environment and thus it is obvious to design the course to resemble a project in a company. This is done by welcoming the students to the virtual company “RealIC Inc.” and stating that the teacher is the manager and the students are the employees.

The students are told that a manager in the industry does not always know the answers nor has the time to assist in all aspects of the development tasks and problems the employees will encounter. This helps set the scene for student learning with respect to generic engineering competences. Therefore, it is required that the students take on the responsibility for their own design and learn to work with problem solving and decision making on their own, mainly using the teacher for sparring and coaching when doing so. The TMs and TAs are planned to support this.

As an example of improving the skills to search for relevant information the students are in the beginning of the course told where the IC process information is located. As the IC process has many different options the students are required to read through the documentation to find the relevant information.

#### *D. The Teaching Method and Activities*

Based on the idea of running the course as a project in a company it was obvious to base the course on project and problem based learning. The students were handed a one page specification for an operational amplifier and requested to deliver a layout ready for manufacturing 3 weeks later.

The teaching activities are planned to support the ILOs and the development of the generic engineering competences. Six different teaching activities are planned: pre-test, lectures, status meetings, a review meeting, coaching sessions and computer work. In Table I the TAs (except the pre-test) and the ILOs are mapped. The status meetings and review meeting are used in the course as these probably are the most common types of meetings used in the industry.

The pre-test is given to the student in the morning at the first day of the course. The test is formed as a multiple choice quiz with 20 questions that test the pre-requisites of the course. Based on the results of the pre-test the students are grouped in pairs with approximately the same level of skills. Besides from matching the students the pre-test also helps to

determine the need for extra lectures to cover weak spots in the students’ background knowledge.

The lectures in the course are basically introductory lessons to various topics. The lectures are aligned with the progress of the students’ work, e.g., an introduction to layout is given at the time where the students are ready to begin layout. All the lectures are short and cover only the most basic aspects of the topic. It is then expected that the students continue learning as they work with the topic.

Two times every week a status meeting is held where all the students are requested to present a very short status on their design and findings, as well as highlight the challenges and tasks they will focus on until the next status meeting. The project manager makes notes on the discussions and identifies action points which are listed and sent out after the meeting. The main purpose of the meeting is to motivate the students to discuss their problems and share experiences and thereby self-assess their work. Therefore, it is important that the teacher intervenes as little as possible to leave room for the students to discuss. As a teacher these meetings are also a valuable help to identify where the students need guidance and to identify topics where extra lectures are needed.

Half way through the course a review meeting is held. In a 20 minutes presentation the students are requested to present the status of their design in detail and the design considerations for the remaining time of the course. After the presentation the other groups are requested to review what has been presented and thereby provide the group under review valuable information before proceeding. Again, the role of the teacher is to do notes and list action points and only at the end of the session share his observations. To facilitate a good review meeting a lecture was given by a manager from an external company on how they do review, but more importantly also to teach what good behavior and practice during a review meeting is.

The goal of the course being the design of an integrated circuit means that the student should have as much time for practical computer work as possible. The EDA tools for IC design are complex and require hand-on exercises to learn. Thus, all lectures, status meetings and the review meeting were kept short and held in the morning, leaving most of the day for design and computer work. The lectures are concentrated in the first 1½ weeks of the course as the time required for computer work intensifies as the course progresses.

The last and perhaps most important teaching activity is the coaching sessions. Each day during the course the teacher meets with each group to discuss their current challenges. To assist the students two techniques were used; coaching and problem solving. The students are introduced to the 4 steps problem solving methodology shown in Fig. 4 (simplified from the 7 step model used by the US Army [9]). The students are requested to work with their problem using the model before addressing the teacher. In this way the students are to present their ideas and views of the problem and possible solutions. The teacher mainly helps making sure that all alternatives are covered and that the solution the students

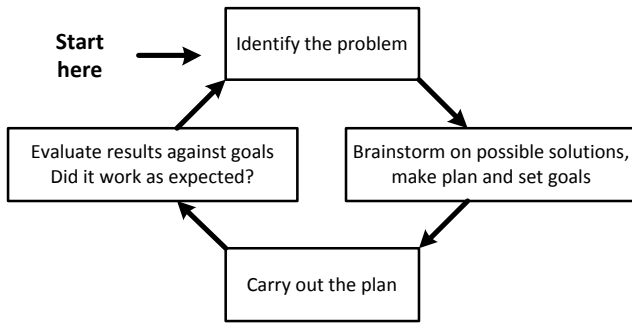


Fig. 4. Problem solving methodology simplified from [9].

choose is based on good argumentation. When using this methodology it is important to support the solution that the students choose rather than focus on them finding the best solution. This increase student learning and not least ensure ownership of their design.

#### E. Assessment

The main concern in the planning of the course is to create an environment where the student feels safe to participate in all the activities planned in the course, as this was mandatory for a success of the course. Therefore, the students are only assessed on a final written report and graded passed or failed. It is also clearly communicated that the students are not assessed on their performance during the course and that it is a natural part of development to make mistakes as long as one learns from these. The latter being supported by examples from the industry.

Assessing generic engineering competences is not as straightforward as assessing technical skills as these are difficult to measure objectively. This is also the reason for them not being incorporated in the ILOs. To provide the students feedback on the generic engineering competences a 4 step feedback method for formative feedback, very similar to the DESC (Describe – Express – Specify – Consequence) [10], [11], is used:

1. **Describe** the observed behavior/situation to the student
2. **Express** how it makes one feel (the impact is has on me)
3. Communicate the **consequence** of the behavior.
4. **Suggest:**
  - a. a new behavior (developing feedback, change this)
  - b. a continued behavior (positive feedback, more of this)

Note that the feedback method is used for both positive and developing feedback and that it is equally important to provide both kinds of feedback. It goes beyond the scope of this paper to discuss good feedback culture in detail but a feedback should be provided soon after the observation while the situation is fresh in memory. It must be kept in a constructive tone and one must always make sure the student is aware that a feedback is given. A feedback should not last for more than 2-3 minutes.

TABLE II. THE AVERAGE SCORE FROM THE CEQ

| Category                       | Average (1 -5) |
|--------------------------------|----------------|
| Good teaching (GT)             | 4.37           |
| Clear Goals and Standards (CG) | 4.07           |
| Appropriate Workload (AW)      | 3.78           |
| Generic Skills (GS)            | 4.17           |
| Motivation (M)                 | 4.83           |
| <b>Overall</b>                 | <b>4.28</b>    |

#### F. Course Evaluation

At the end of the course the learning of the students was evaluated using the Course Experience Questionnaire (CEQ) [12]. Through 22 questions the students evaluated the course in the five categories listed in Table II, “1” and “5” being the lowest and highest score, respectively. In addition to the questions the students are also asked to state what they find to be good and what could be done to improve the course. The CEQ is based on answers from 6 students who completed the course (2 students dropped out of the course after only one week) and the average scores are shown in Table II.

In general all the scores are very good. The lowest score is the category Appropriate Workload (AW) = 3.78. Looking at the answers to the questions in this category it is clear that the reason for the relatively low score is that many topics were covered and also that it is hard for the student to know when their design is completed. However, some students also suggested that the course could be improved by covering more topics. Also, the very high score in the category Motivation (MS) = 4.83 shows that the students were highly motivated by the course and thus also motivated to learn more even though the workload in the course was already high.

The average score for the Clear Goals and Standards (CG) is 4.07, which is quite high but still the second lowest score. The reason for this relatively low score is most likely related to the coaching approach used in the course where the main idea is not always to provide straight answers. In one case one group of students decided to solve a problem in a certain way which was approved by the teacher. After two days the students realized that the proposed idea did not solve the problem. The students were very frustrated when realizing that the teacher knew that the proposed idea most likely did not work. After a discussion between the students and the teacher the students realized that they probably learned significantly more compared to a situation where the teacher had just suggested a solution. In another situation one group came up with a solution that turned out to be better than the one that the teacher would have proposed, clearly illustrating the strength of the coaching technique and the importance of not providing immediate solutions. Keeping in mind that the main objective of the course is for the students to learn rather than reaching a perfect design clearly justifies using coaching when guiding the students. However, during the first week some students were very frustrated that their questions were not answered directly, but as the course progressed and the students began to develop their circuit their satisfaction

increased drastically as they clearly felt that they made all the decisions.

The students clearly appreciate the teaching method and activities as the Good Teaching (GT) = 4.37 and the generic engineering competence is strongly improved GS = 4.17. Especially, the status meeting turned out a great success. As the teacher was engaged doing the notes the students quickly realized that the discussions had to take place among themselves. The discussion flourished and the students discussed and brainstormed about their problems. For the teacher it turned out that the strongest tool was to keep quiet while letting the students finish their discussions. After the discussions ended the teacher provided his view on various topics and occasionally made short (less the 15 minutes) ad-hoc lectures.

The review meeting was also highly appreciated by the students and the informal environment from the status meeting was also present in this meeting. The success of the review meeting would probably have been much lower if not for the status meetings where the open minded culture and positive atmosphere was founded. The students clearly felt the value for themselves in both the status and review meeting.

By creating an informal atmosphere in both the status meetings and the review meeting the students self-assessed their work providing both criticism and recognition of their respective designs. Finally, it was a general comment from most of the students that running the course using the company model was very inspiring to them.

#### G. Future Improvements

From the comments from the students a few topics were highlighted for future improvement to the course.

More lectures given by external lecturers are requested. In general the students appreciate all sort of information about being an engineer in the industry.

Even though the students in the CEQ rate the workload as above average for the course, many students requested that more topics like parasitic extraction, Monte Carlo and noise simulations are covered in the course. These topics could be covered in the course by letting each group get an individual topic, learn it and then teach it to the other students. An alternative is to incorporate these topics in the second new course where the students are to perform measurements on their devices and correlate these with simulations.

In case more students will attend the course in the future the course structure can be maintained by splitting the students up in different project groups. I.e., the students are divided into teams of maximum 10 students each having their own status meeting etc., the only penalty being the extra effort needed by the teacher.

#### V. CONCLUSIONS

A strategy has been presented for planning the sequence of courses in integrated analog electronics that offers the students the opportunity to design, layout and tape-out a circuit and after fabrication perform measurements on their circuit. It has briefly been described how a course can be designed using

constructive alignment based on intended learning objective, teaching activities and assessment. The methodology for designing a course has been illustrated in detail by describing how the first of two new courses is designed. The primary objective of the course is to teach the students the flow that an IC designer must go through when doing analog integrated circuit design. The secondary objective of the course is to strengthen the generic engineering competences of the students. To support these two objectives the course is run like a project in a company with status meetings and a review meeting where the student self-assess their work. The course was evaluated using the Course Evaluation Questionnaire (CEQ) and showed excellent results with an overall average score of 4.28 out of 5. Especially, the teaching activities and the motivation had very high scores indicating that the students appreciate the company setup. Finally, a few suggestions on how to improve the course were discussed.

#### VI. ACKNOWLEDGEMENT

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